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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/736,724	12/13/00	YAMAZAKI S	07977-175002

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EXAMINER	
BROCK II,P	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/01/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/736,724	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- Th MAILING DATE of this communication appears on th cov r sh et with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/912,979* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3 – 6, 11 – 12, 17 and 65 – 67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear how a "groove-like pattern" can form a "dotted pattern" when filled with thermal oxide.

3. Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by "artificially and locally forming impurity regions by addition of impurity elements... in the channel forming region" and then countering the statement by saying "wherein the impurity elements are not added or are added by a very small amount in a region other than the impurity regions in the channel forming region". It is not clear if there are impurity elements added to the channel forming region.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 9, 10, 18 – 24, 26, 29, 30, 32, 35 – 37, 39, 42 – 44, 46, 49 – 51, 53, 56, 57, 58, 60, 63 and 64 are rejected under 35 U.S.C. 102(e) as being anticipated by Mase et al. (USPAT 6236064, Mase).

Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 a method of manufacturing an insulated gate semiconductor device.

With regard to claim 9, Mase discloses in column 5, lines 27 – 40 introducing a first impurity into a crystal semiconductor having a part to become a channel forming region to form a plurality of impurity regions which inherently form a dotted pattern in the part to become the channel forming region as viewed from above the part to become the channel forming region toward a direction of depth of the channel forming region, the plurality of impurity regions containing an oxygen as the first impurity. Mase discloses in figures 5a – 5c introducing into the crystal semiconductor (52) a second impurity that gives one conductivity to form a source region and a drain region (415 and 412) in the crystal semiconductor with the channel forming region (414) therebetween.

With regard to claim 10, Mase discloses in figures 5a – 5c forming a gate insulating film (420) over the part to become the channel forming region inherently after the step of introducing the first impurity. Mase discloses in figures 5a – 5c forming a gate electrode (416) over the part to become the channel forming region with the gate insulating film therebetween.

With regard to claim 18, Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a source region, a drain region and a channel forming region using a crystal semiconductor. Mase discloses in figures 5a – 5c forming a gate insulating film and a gate electrode on the channel forming region. Mase inherently discloses in the channel forming

region, forming a region in which carriers move, and impurity regions which pin a depletion layer that expands from the drain region toward the channel forming region and the source region, artificially and locally.

With regard to claim 19, Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a source region, a drain region and a channel forming region using a crystal semiconductor. Mase discloses in figures 5a – 5c forming a gate insulating film and a gate electrode on the channel forming region. Mase inherently discloses in the channel forming region, forming a region in which carriers move, and impurity regions which control the threshold voltage to a predetermined value voltage by the addition of impurity elements, artificially and locally.

With regard to claim 20, Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a source region, a drain region and a channel forming region using a crystal semiconductor. Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming impurity regions artificially and locally in the channel forming region. Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a gate insulating film and a gate electrode on the channel forming region. Mase inherently discloses wherein impurity elements that expand an energy band width are artificially and locally added to the impurity regions.

With regard to claim 21, Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a source region, a drain region and a channel forming region using a crystal semiconductor. Mase discloses in figures 5a – 5c forming a gate insulating film and a gate electrode on the channel forming region. Mase inherently discloses in order to form impurity regions which pin a depletion layer that expands from the drain region toward the channel

forming region and the source region, artificially and locally adding impurity elements that expand an energy band width to the channel forming region.

With regard to claim 22, Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a source region, a drain region and a channel forming region using a crystal semiconductor. . Mase discloses in figures 5a – 5c forming a gate insulating film and a gate electrode on the channel forming region. Mase inherently discloses in order to form impurity regions which control the threshold voltage to a predetermined value voltage by addition of impurity elements, artificially and locally adding impurity elements that expand an energy band width to the channel forming region.

With regard to claim 23, Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a source region, a drain region and a channel forming region using a crystal semiconductor. Mase inherently discloses artificially and locally forming impurity regions by addition of impurity elements that expand an energy band width in the channel forming region. Mase discloses in figures 5a – 5c forming a gate insulating film and a gate electrode on the channel forming region. It is inherent in the method of Mase wherein the impurity elements have an insulating property. Mase discloses in column 5, lines 27 – 40 wherein the impurity elements are not added or are added by a very small amount in a region other than the impurity regions in the channel forming region.

With regard to claims 24, 30, 37, 44, 51 and 58, it is inherent in the method of Mase that a region other than the impurity region within the channel forming region is an intrinsic region.

With regard to claims 26, 32, 39, 46, 53 and 60, it is inherent in the method of Mase wherein at least one section perpendicular to a channel direction of the channel forming region is

substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by the impurity regions.

With regard to claims 29, 35, 42, 49, 56 and 63, it is inherent in the method of Mase wherein the impurity regions are in a dot pattern.

With regard to claims 36, 43, 50, 57 and 64, Mase discloses in column 5, lines 27 – 40 wherein the impurity elements are oxygen.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mase in view of Mukai et al. (USPAT 5585658, Mukai).

With regard to claim 1, it is inherent in the method of Mase that in order to implant ions into only parts of the channel formation region a mask has to be formed over a crystal semiconductor comprising a part to become a channel forming region. Further it is inherent in the method of Mase that a dotted hole would have to be formed in the mask. Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a plurality of impurity regions which inherently form a dotted pattern in the part to become the channel forming region as viewed from above the part to become the channel forming region toward a direction of depth of the channel forming region, the step of forming the plurality of impurity regions being conducted by

introducing a first impurity thereinto having the dotted hole, the first impurity being oxygen. Mase also discloses in figures 5a – 5c and column 5, lines 27 – 40 introducing into the crystal semiconductor a second impurity that gives one conductivity to form a source region and a grain region in the crystal semiconductor with the channel forming region therebetween. It is inherent in the method of Mase that the impurity regions are formed through a mask over a crystal semiconductor. Mase does not disclose that the impurity region is formed through a resist mask with a dotted pattern that is patterned by the focused ion beam (FIB) method. Mukai discloses in figures 3a – 3e forming a resist mask (16) and patterning (17) the resist mask by using FIB method (18). It would have been obvious to one of ordinary skill in the art to use the resist and patterning using the FIB method of Mukai in the method of Mase in order to optimally control an impurity profile as discussed by Mukai in column 1, lines 54 – 58.

With regard to claim 2, Mase discloses in figures 5a – 5c forming a gate insulating film over the part to become the channel forming region after the step of forming the plurality of impurity regions. Mase discloses in figures 5a – 5c forming a gate electrode over the part to become the channel forming region with the fate insulating film therebetween.

7. Claims 7 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (JPPAT 404186775a, Yamazaki).

With regard to claim 7, Yamazaki discloses in figures 1a – 1d implanting an oxygen ion into a crystal semiconductor (2) comprising a part to become a channel forming region. Yamazaki does not disclose a method of electron beam to implant the oxygen ion. Yamazaki discloses thermally treating the crystal semiconductor comprising silicon to change a region

thereof implanted with the oxygen ion by the implanting step into an oxide region which inherently forms a dotted pattern in the part to become the channel forming region viewed from above the part to become the channel forming region toward a direction of depth of the channel forming region. Yamazaki discloses in figure 1c introducing into the crystal semiconductor an impurity that gives one conductivity to form a source region (6) and a drain region (5) in the crystal semiconductor with the channel forming region (7) therebetween. It is well known in the art to implant an oxygen ion into a crystal semiconductor by electron beam. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use electron beam to implant oxygen ion in order to increase the concentration of ions in the semiconductor crystal.

With regard to claim 8, Yamazaki discloses in figure 1b forming a gate insulating film (3) over the part to become the channel forming region after the step of introducing the first impurity. Yamazaki discloses in figure 1b forming a gate electrode (4) over the part to become the channel forming region with the gate insulating film therebetween.

8. Claims 15 – 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (JPPAT 404186775a, Yamazaki) in view of Mukai.

With regard to claim 15, Yamazaki discloses in figures 1a – 1d forming a resist over a crystal semiconductor comprising a part to become a channel forming region. Yamazaki discloses in figures 1a – 1d forming a hole that is inherently dotted in the resist by patterning the resist. Yamazaki does not disclose patterning the resist by and FIB method. Mukai discloses in

figures 3a – 3e forming a resist mask (16) and patterning (17) the resist mask by using FIB method (18). It would have been obvious to one of ordinary skill in the art to use the resist and patterning using the FIB method of Mukai in the method of Yamazaki in order to optimally control an impurity profile as discussed by Mukai in column 1, lines 54 – 58. Yamazaki discloses in figures 1a – 1d forming a plurality of impurity regions which inherently form a dotted region as viewed from above the part to become the channel forming region toward a direction of depth of the channel forming region, the step of forming the plurality of impurity regions being conducted by intruding a first impurity thereinto through the resist having the dotted hole, the first impurity being oxygen. Yamazaki discloses in figures 1a – 1d introducing into the crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in the crystal semiconductor with the channel forming region therebetween. Yamazaki discloses in figures 1a – 1d wherein the dotted pattern has an arrangement in which the impurity regions form one row extending in a direction of a channel length of the channel forming region.

With regard to claim 16, Yamazaki discloses in figure 1b forming a gate insulating film (3) over the part to become the channel forming region after the step of introducing the first impurity. Yamazaki discloses in figure 1b forming a gate electrode (4) over the part to become the channel forming region with the gate insulating film therebetween.

9. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mase.

With regard to claim 13, Mase discloses in column 5, lines 27 – 40 introducing a first impurity into a crystal semiconductor having a part to become a channel forming region to form a plurality of impurity regions which inherently form a dotted pattern in the part to become the

channel forming region as viewed from above the part to become the channel forming region toward a direction of depth of the channel forming region, the plurality of impurity regions containing an oxygen as the first impurity. Mase discloses in figures 5a – 5c introducing into the crystal semiconductor (52) a second impurity that gives one conductivity to form a source region and a drain region (415 and 412) in the crystal semiconductor with the channel forming region (414) therebetween. Mase does not disclose intervals and impurity regions that alternate with the intervals in a direction of a channel width of the channel forming region. It is well known in the art to space regions into intervals wherein there are could be 1 to 9 regions and 1 to 9 intervals between the regions in the direction of a channel width, and that would mean that impurity regions can have a total width of W_{pi} in a direction of a width W, and a total of the intervals in W_{pa} in a direction of the width, wherein $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use spacing of the intervals in an orderly manner such as 1 to 9 impurity regions and 1 to 9 interval in the method of Mase in order to have a set pattern which can be formed in a grid like fashion.

With regard to claim 14, Mase discloses in figures 5a – 5c forming a gate insulating film over the part to become the channel forming region after the step of forming the plurality of impurity regions. Mase discloses in figures 5a – 5c forming a gate electrode over the part to become the channel forming region with the fate insulating film therebetween.

10. Claims 25, 31, 38, 45, 52 and 59 27, 33, 40, 47, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mase as applied to claims 18 – 23 above, respectively, and further in view of one of ordinary skill in the art.

With regard to claims 25, 31, 38, 45, 52 and 59, Mase does not disclose intervals and impurity regions that alternate with the intervals in a direction of a channel width of the channel forming region. It is well known in the art to space regions into intervals wherein there are could be 1 to 10 regions and 1 to 10 intervals between the regions in the direction of a channel width, and that would mean that impurity regions can have a total width of W_{pi} in a direction of a width W, and a total of the intervals W_{pa} in a direction of the width, wherein $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use spacing of the intervals in an orderly manner such as 1 to 10 impurity regions and 1 to 10 intervals in the method of Mase in order to have a set pattern which can be formed in a grid like fashion.

With regard to claims 27, 33, 40, 47, 54 and 61, Mase does not disclose intervals and impurity regions that alternate with the intervals in a direction of a channel width of the channel forming region. It is well known in the art to arrange regions at intervals of 100 to 3000 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use spacing of 100 to 3000 Å for the impurity regions of Mase in order for each impurity region to be isolated from each other.

With regard to claims 28, 34, 41, 48, 55, and 62, Mase does not disclose that the crystal semiconductor is a monocrystal semiconductor. It is well known in the art to have a monocrystal semiconductor instead of a polycrystal or amorphous semiconductor. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use a monocrystal semiconductor as the crystal semiconductor in the method of Mase in order to have superior electrical characteristics of the gate electrode.

Allowable Subject Matter

11. Claims 3 – 6, 11 – 12, 17 and 65 – 67 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

12. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record either singularly or in combination do not disclose or suggest at least the step of etching portions of a channel forming region and then implanting those regions with oxygen, carbon, or nitrogen.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Walden, Fujiwara et al., Yamaguchi et al. and Kato all disclose FIB. Mitsui discloses patterning dots. Goto et al. and Harriott et al. both disclose patterning by ion beam.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
July 27, 2001

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